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Bias stress effect in low-voltage organic thin-film transistors

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Abstract The bias stress effect in pentacene organic thin-film transistors has been investigated. The transistors utilize a thin gate dielectric based on an organic self-assembled monolayer and thus can be operated at low voltages. The bias stress-induced threshold voltage shift has been analyzed for different drain-source voltages. By fitting the time-dependent threshold voltage shift to a stretched exponential function, both the maximum (equilibrium) threshold voltage shift and the time constant of the threshold voltage shift were determined for each drain-source voltage. It was found that both the equilibrium threshold voltage shift and the time constant decrease significantly with increasing drain-source voltage. This suggests that when a drain-source voltage is applied to the transistor during gate bias stress, the tilting of the HOMO and LUMO bands along the channel creates a pathway for the fast release of trapped carriers.

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1 Introduction

When a carrier channel is created in a field-effect transistor by applying a gate-source voltage, the threshold voltage of the transistor changes over time. This phenomenon is known as bias stress effect. Applying a negative gate-source voltage to a p-channel transistor causes its threshold voltage to shift towards more negative values, while a positive gate-source voltage applied to an n-channel transistor induces a positive threshold voltage shift. The bias stress effect is attributed to the trapping of carriers from the gate bias-induced conduction channel into localized (i.e., less mobile) electronic states. These trap states may be located within the semiconductor, at the semiconductor/dielectric interface, or in the gate dielectric. The longer the gate bias is applied, the more carriers are trapped, and hence the larger is the shift in threshold voltage. The trapped carriers still contribute to the charge balance in the transistor, but not to the drain current, and this manifests itself as a shift in threshold voltage. As a result, the number of mobile charges and hence the drain current at a given gate-source voltage decrease over time. Depending on the physical characteristics of the trap states, trapped carriers either return to mobile states after the gate-source voltage is removed, or they remain trapped until the trap states are physically eliminated, for example, by thermal annealing.

The bias stress effect may also be observed when a transistor is biased deeply into the off-state (i.e., when a positive gate-source voltage is applied to a p-channel transistor, or a negative gate-source voltage is applied to an n-channel transistor). In this case, carriers initially located in trap states are released into mobile states, and this will shift the threshold voltage into the direction of the applied gate-source voltage.

The physical mechanisms of the carrier trapping and release processes depend on the materials employed for the semiconductor and gate dielectric. In the case of thin-film transistors (TFTs) with hydrogenated amorphous silicon (a-Si:H) as the semiconductor and amorphous silicon nitride as the gate dielectric (both deposited by plasma-enhanced chemical vapor deposition at temperatures around 200 to 300°C), initial studies suggested that carriers are trapped

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in the silicon nitride gate dielectric [1]. Later it was discovered that the bias stress also modifies the a-Si:H microstructure by creating unsaturated valence states into which electrons are trapped [2–4]. Carriers trapped in a-Si:H remain trapped after the gate bias has been removed. To reverse the bias stress-induced threshold voltage shift, the structural defects in the a-Si:H must be annealed at a temperature above 180°C [5, 6].

In contrast, the bias stress-induced threshold voltage shift in organic TFTs is usually not persistent, i.e., carriers trapped during bias stress are released more or less rapidly after the gate-source voltage has been removed, without the need for thermal annealing. A number of studies have shown that the bias stress effect in organic TFTs is independent of the gate dielectric material and its quality, from which it was concluded that the bias stress-induced carrier trapping in organic TFTs occurs only in the semiconductor and not in the gate dielectric or at the semiconductor/dielectric interface [7–9]. However, changing the gate dielectric and/or the properties of the semiconductor/dielectric interface usually affects the growth of the organic semiconductor and in particular the morphology of the first few monolayers of the semiconductor, which makes it difficult to distinguish between interface and volume effects and to entirely rule out that trapping occurs at the semiconductor/dielectric interface.

The microscopic mechanism of the bias stress effect in organic semiconductors has not been conclusively determined. For the semiconducting polymers poly(9,9′-dioctylfluorene-co-bithiophene) (F8T2) and regioregular poly(3-hexylthiophene) (P3HT), Street, Salleo, and Chabinyc [9] proposed the formation of hole bipolarons as the mechanism responsible for the stress-induced threshold voltage shift, based on the observation that the number of carriers trapped per time and area is proportional to the square of the gate bias-induced carrier concentration in the channel. Gomes et al. [10] reported an anomaly in the temperature-dependence of the drain current of TFTs based on P3HT, poly(arylamine), and sexithiophene (6T) and thus ascribed the bias stress effect to the presence of water in the semiconductor film. This hypothesis is supported by the observation that the bias stress effect in TFTs based on vacuum-deposited pentacene films can be reduced by protecting the transistors against ambient humidity, either with an encapsulation layer [11] or by operating the transistors in vacuum [12]. Also, Goldmann et al. [13] showed that bias stress-induced trap formation in pentacene single-crystal transistors is significantly reduced when the gate dielectric is rendered hydrophobic with the use of a self-assembled monolayer. Recently, Wang et al. [14] reported that the shift in threshold voltage during bias stress in pentacene TFTs is accompanied by an increase in contact resistance, from which the authors concluded that some of the trapping occurs in states located in the vicinity of the source and drain contacts, as opposed to states at or near the semiconductor/dielectric interface.

2 Theory

The time-dependence of the bias stress-induced threshold voltage shift under a constant gate-source voltage and a constant drain-source voltage is typically described by a stretched exponential function [15, 16]:

$$\Delta V_{\mathrm{th}}(t) = \left[V_{\mathrm{th}}(\infty) - V_{\mathrm{th}}(0)\right]\left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \tag{1}$$

where $V_{\mathrm{th}}(0)$ is the threshold voltage in the virgin state, $V_{\mathrm{th}}(\infty)$ is the threshold voltage when equilibrium has been reached at $t \rightarrow \infty$, τ is the time constant, and β is the stretching parameter ($0 < \beta \leq 1$). The stretched exponential function is an empirical function that was introduced by Rudolf Kohlrausch in 1854 to describe the time-dependent discharge of capacitors [17], and hence it is sometimes referred to as the Kohlrausch function [18]. Although empirical, the stretched exponential function is useful to describe time-dependent processes that are inherently exponential, but occur in complex systems that are characterized by a distribution of local environments giving rise to a distribution of time constants. The result of this distribution of time constants is a faster-than-exponential response early in the process (for times up to the time constant τ) and a slower-than-exponential response later in the process (for times beyond the time constant τ), i.e. a stretched exponential function [18].

The degree of diversion from the exponential function is described by the stretching parameter β. A stretching parameter close to 1 indicates a narrow distribution of time constants (the limit $\beta = 1$ being the exponential function with a single time constant), while a smaller stretching parameter ($\beta < 1$) implies a broader distribution of time constants. Regardless of β, the parameter τ in (1) indicates the time at which the function value has reached 63% of the equilibrium value expected for $t \rightarrow \infty$. However, because the stretching leads to a slower-than-exponential response for times beyond τ, a stretched exponential function takes longer to approach equilibrium than an exponential function, depending on the value of β. In other words, the time until 90%, 95% or 99% of the equilibrium value is reached is much longer when $\beta \ll 1$. To simplify comparisons between exponential and stretched exponential functions, it is useful to characterize the stretched exponential function by an average time constant that takes into account the stretching parameter β [18]:

$$\langle \tau \rangle = \int_0^{\infty} e^{-\left(\frac{t}{\tau}\right)^{\beta}} dt = \frac{\tau}{\beta} \cdot \Gamma\left(\frac{1}{\beta}\right), \tag{2}$$

where $\Gamma(z)$ is Euler's gamma function, i.e., a generalized factorial function.

How fast the threshold voltage shifts during gate bias stress depends on the applied gate-source and drain-source voltages. A larger gate-source voltage leads to a faster threshold voltage shift [5], presumably because a larger gate-source voltage induces a larger density of charge carriers in the channel, which at a constant trapping rate increases the number of carriers trapped per time and area [9, 19]. A larger drain-source voltage, on the other hand, leads to a *slower* bias stress-induced threshold voltage shift [19]. This observation has been attributed to the fact that a larger drain-source voltage counteracts the electrical field generated by the gate-source voltage near the drain contact, thereby decreasing the carrier density in the channel close to the drain contact and thus reducing the number of carriers trapped per time and area [19]. However, our experimental results shown below suggest that the reduction in threshold voltage shift with increasing drain-source voltage can also be explained by the enhanced release of trapped carriers as a result of the lateral electrical field along the channel created by the drain-source voltage.

3 Experimental

With few exceptions [20], bias stress effect measurements have been reported for transistors that employ relatively thick gate dielectrics and thus require relatively large gate-source voltages, usually greater than 10 V. Here we utilize a very thin gate dielectric with a thickness of 5.7 nm and a capacitance of 0.7 $\mu F\,cm^{-2}$, so that a gate-source voltage of 3 V is sufficient to induce a carrier density of about 10^{13} cm^{-2} in the channel [21]. The TFTs were manufactured on glass substrates using an inverted staggered (bottom-gate, top-contact) transistor structure (see Fig. 1a). To prepare the gate electrodes, aluminum was deposited through a shadow mask to a thickness of 20 nm. After the aluminum deposition the substrate was briefly exposed to an oxygen plasma (to create a thin hydroxyl-terminated layer of aluminum oxide) and then immersed in a 2-propanol solution of n-octadecylphosphonic acid (to allow a molecular monolayer to self-assemble on the oxidized aluminum gate electrodes). After about 16 hours, the substrate was removed from the solution, blown dry in a stream of nitrogen, and briefly baked on a hotplate at 60°C. Thus, the gate dielectric consists of a 3.6-nm-thick aluminum oxide film and a 2.1-nm-thick organic monolayer. For the organic semiconductor, a 30-nm-thick film of pentacene (purified by temperature-gradient sublimation) was deposited in vacuum. During the pentacene deposition, the substrate was held at a temperature of 60°C. Finally, 30-nm-thick gold source/drain contacts were deposited by evaporation in vacuum. The metal and semiconductor layers were patterned using polymer shadow masks that were manually aligned under an optical microscope. The transistors have a channel length of 30 µm and a channel width of 100 µm. All electrical measurements were carried out at room temperature

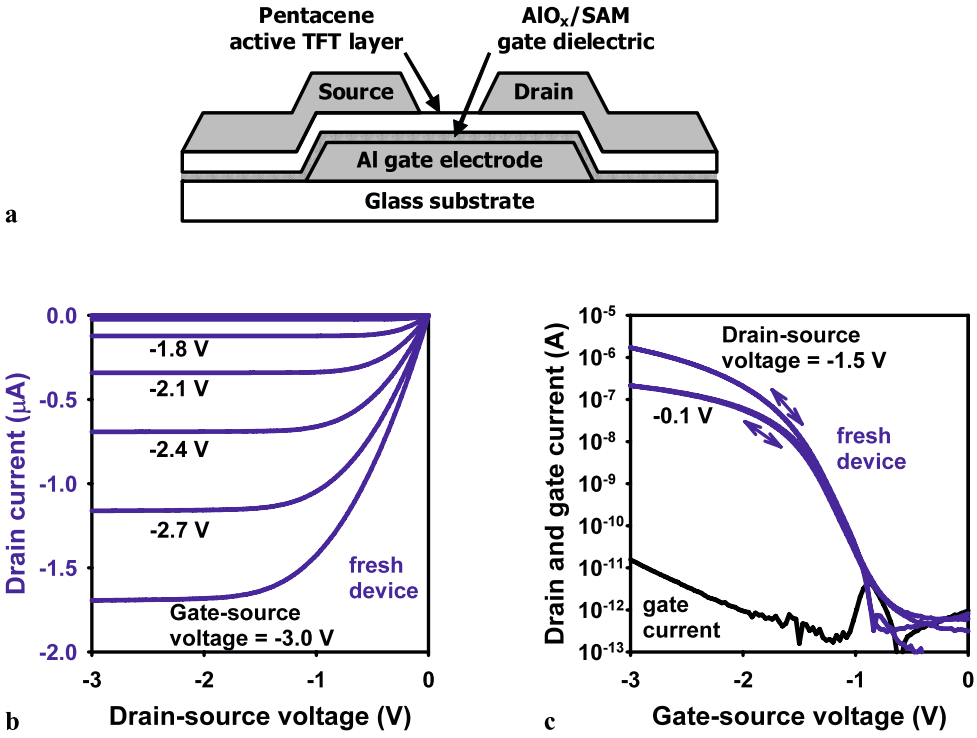

Fig. 1 **a** Schematic cross-section of the transistors. **b** Output characteristics of a pentacene transistor before bias stress. **c** Transfer characteristics of the same transistor before bias stress

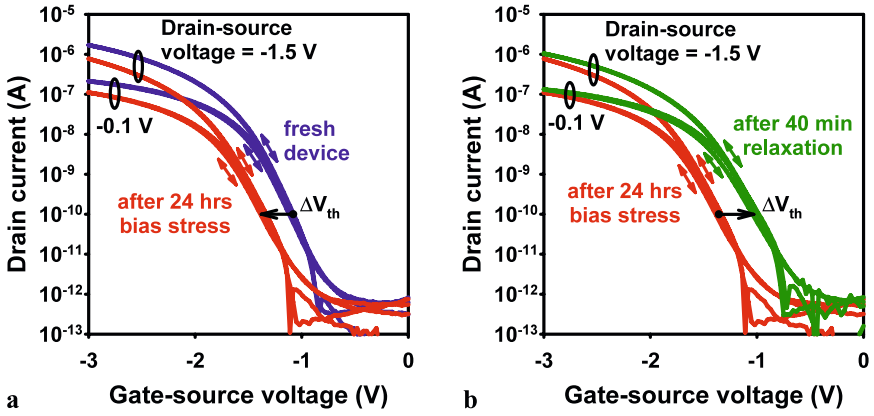

Fig. 2 **a** Transfer characteristics for drain-source voltages of −0.1 and −1.5 V before and after bias stress. During bias stress, a constant gate-source voltage of −3 V and a constant drain-source voltage of −3 V were applied for a period 24 hours. As a result of the bias stress, the threshold voltage (defined as the gate-source voltage at which the drain current is 100 pA) has shifted from −1 V to −1.3 V. The gate current is unaffected by the bias stress experiments. **b** Transfer characteristics of the same transistor after bias stress and after relaxation. During relaxation, no bias was applied for 40 min, and the threshold voltage shifted from −1.3 V back to −1 V

in ambient air under yellow laboratory light. The threshold voltage was extracted from a current-voltage measurement performed over a small bias range and with a fast sweep rate, so that the measurement was completed within five seconds (a time much shorter than the shortest stress time).

4 Results

Figures 1b and 1c show the output and transfer characteristics of a pentacene TFT immediately after fabrication ("fresh device"). For the purpose of the bias stress measurements discussed here, we define the threshold voltage as the gate-source voltage at which the drain current is 100 pA. This definition differs from the definition of the threshold voltage for silicon metal–oxide–semiconductor field-effect transistors, where the threshold voltage is defined as the onset of strong inversion [22]. This concept is not applicable to organic TFTs which normally operate in accumulation mode. Alternatively, the threshold voltage is often defined as the voltage at which the linear fit of the square-root of the drain current plotted versus the gate-source voltage intercepts the gate-source voltage axis. However, since the carrier mobility in organic TFTs is usually a function of the gate-source voltage, fitting the square-root of the drain current is often ambiguous [23–25]. In contrast, when the threshold voltage is defined as the gate-source voltage at a certain drain current in the subthreshold regime, the extraction procedure is unambiguous [26]. In addition, the measurement required to find the gate-source voltage at a certain drain current is relatively quick and therefore does not significantly disturb the bias stress-induced threshold voltage shift. According to our definition, the fresh device in Fig. 1b, c has a threshold voltage of −1 V, regardless of the drain-source voltage.

Figure 2a shows the transfer characteristics of the same transistor before and after stressing with a constant gate-source voltage of −3 V and a constant drain-source voltage of −3 V for 24 hours. The gate-source voltage of −3 V corresponds to a gate field of 5 MV/cm and is a typical operating voltage for integrated circuits based on this device technology [21]. As a result of the 24-hour bias stress, the threshold voltage has shifted from −1 V to −1.3 V. After the stress measurement the transistor was left to relax at room temperature without strong illumination (only in the presence of a relatively weak yellow laboratory light) for 40 minutes, with gate, drain, and source floating. Figure 2b shows that within 40 minutes the threshold voltage returned to its initial value of −1 V.

Figure 3a shows the saturation field-effect mobility of the transistor as a function of gate-source voltage before and after the 24-hour bias stress and after the 40-minute relaxation. During the 24-hour bias stress the mobility decreased from 0.6 $cm^2/V\,s$ to 0.4 $cm^2/V\,s$. For comparison, the mobility of pentacene TFTs left aging in ambient air for 24 hours with the terminals floating degrades by approximately the same amount (see Fig. 3b). This suggests that the mobility degradation during the 24-hour bias stress is mostly due to environmental effects [27] and is not necessarily accelerated by the applied gate-source voltage.

To evaluate the time evolution and the drain-source voltage dependence of the bias stress-induced threshold voltage shift we have performed 28 stress measurements with different stress times (between 30 seconds and 24 hours) and different drain-source voltages (V_{DS} between 0 and −2 V). To avoid ambiguities related to the relaxation process, each measurement was performed on a fresh transistor with identical dimensions. Each measurement consisted of three steps. First, the threshold voltage of the transistor in the vir-

Table 1 Fit parameters obtained by fitting the measured bias stress-induced threshold voltage shifts to (1). Measurement data and fitting lines are shown in Fig. 4. The average time constant $\langle\tau\rangle$ was calculated according to (2). The gate-source voltage during bias stress is −3 V. V_{DS} is the drain-source voltage. R^2 is the coefficient of determination (a measure of the quality of the fit, where R^2 closer to unity represents a better fit)

V_{DS} (V)	$V_{th}(\infty)-V_{th}(0)$	τ (s)	β	$\langle\tau\rangle$ (s)	R^2
0	4.479	1.67×10^7	0.294	1.70×10^8	0.9884
−0.5	2.747	4.84×10^6	0.304	4.22×10^7	0.9992
−1.0	0.759	2.78×10^4	0.393	9.71×10^4	0.9998
−2.0	0.395	4.82×10^3	0.428	1.34×10^4	0.9971

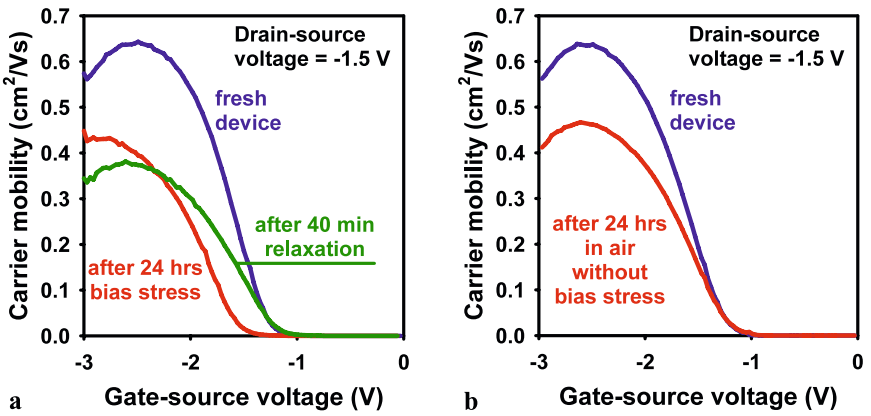

Fig. 3 **a** Saturation field-effect mobility of the transistor from Figs. 1b and 2 as a function of gate-source voltage before bias stress, after bias stress (24 hours at $V_{GS} = -3$ V and $V_{DS} = -3$ V) and after relaxation (40 min without bias). **b** Saturation field-effect mobility of a different pentacene transistor immediately after fabrication and after aging in ambient air for 24 hours with the terminals floating. Note that the rate of mobility degradation is independent of bias stress

gin state was measured. A constant gate-source voltage of −3 V and a constant drain-source voltage of 0, −0.5, −1, or −2 V was then applied for a certain amount of time. Immediately after completion of the bias stress, the threshold voltage of the stressed transistor was measured.

The results of the bias stress measurements are summarized in Fig. 4. The largest threshold voltage shift we have measured is 0.8 V (for $V_{GS} = -3$ V, $V_{DS} = 0$ V and a stress time of 16 hours). The threshold voltage shift obtained for a given stress time was found to decrease monotonically with increasing drain-source voltage, in accordance with the results reported by Zan and Kao [19]. For each drain-source voltage, we have fitted the time-dependence of the measured threshold voltage shift to (1). The fit parameters obtained for each drain-source voltage are summarized in Table 1, along with the average time constant $\langle\tau\rangle$ calculated using (2).

The results show that applying a drain-source voltage during the gate bias stress has two distinct effects on the threshold voltage shift. One is that a larger drain-source voltage reduces the maximum (equilibrium) threshold voltage shift expected for $t \to \infty$. For example, the equilibrium threshold voltage shift is 4.5 V when $V_{DS} = 0$ V, but only 0.4 V when $V_{DS} = -2$ V. The other effect of the drain-source voltage is a significant reduction in the time constant τ. For example, the time constant τ is 193 days when $V_{DS} = 0$ V, as opposed to only 80 minutes when $V_{DS} = -2$ V. In other words, when V_{DS} is increased, the time to equilibrium is significantly reduced. (We note that extrapolating from a maximum stress time of 24 hours to a time constant of 193 days should be taken with care. For a more precise assessment of the threshold voltage shift at small drain-source voltages, the experimental stress times should be significantly increased.)

The stretching parameter β obtained from the fits is between 0.3 and 0.4, which is similar to Ref. [16] (β between 0.4 to 0.42 for pentacene TFTs), Ref. [19] (β of 0.28 for pentacene TFTs), and Ref. [28] (β of 0.44 for poly(triarylamine) TFTs). The results indicate that the stretching parameter β increases slightly with increasing drain-source voltage, from about 0.3 for $V_{DS} = 0$ V to about 0.4 for $V_{DS} = -2$ V.

5 Discussion

The observation that both the equilibrium threshold voltage shift *and* the time constant τ decrease dramatically with increasing drain-source voltage suggests that the drain-source voltage does not only reduce the number of charge carriers available for bias stress-induced trapping (by counteracting the gate field near the drain contact, as suggested by Zan and Kao [19]), but in addition creates a pathway for the fast release of trapped carriers. This detrapping pathway may

Table 2 Calculated times until 90%, 95%, and 99% of the equilibrium threshold voltage shift is reached during bias stress for each drain-source voltage

V_{DS} (V)	τ (s)	$\langle\tau\rangle$ (s)	$t_{90\%}$ (s)	$t_{95\%}$ (s)	$t_{99\%}$ (s)
0	1.67×10^7	1.70×10^8	2.85×10^8	6.97×10^8	3.01×10^9
−0.5	4.84×10^6	4.22×10^7	7.52×10^7	1.79×10^8	7.35×10^8
−1.0	2.78×10^4	9.71×10^4	2.32×10^5	4.53×10^5	1.35×10^6
−2.0	4.82×10^3	1.34×10^4	3.38×10^4	6.26×10^4	1.71×10^5

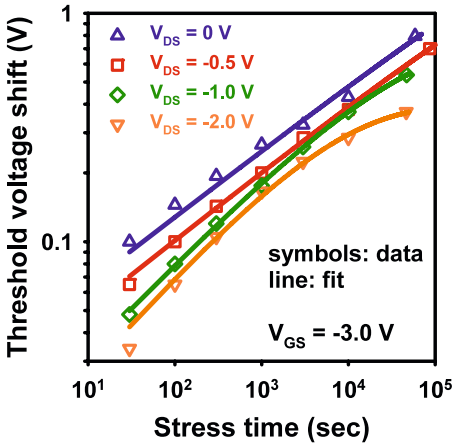

Fig. 4 Bias stress-induced threshold voltage shift as a function of stress time. During bias stress, a constant gate-source voltage of −3 V and a constant drain-source voltage of 0 V, −0.5 V, −1 V, or −2 V were applied. The symbols are experimental data; the lines are numerical fits to the data using (1). The fit parameters are summarized in Table 1

be related to the tilting of the HOMO and LUMO bands that results from the lateral electrical field created by the drain-source voltage along the channel. The band tilting increases with increasing drain-source voltage and reduces the barrier height that carriers trapped in localized states must overcome in order to return to mobile states in the channel; this is known as the Poole–Frenkel effect [26, 29]. When gate bias stress is performed in the presence of a significant drain potential, carriers trapped into localized states are more quickly released back into mobile channel states, and as a result the equilibrium threshold voltage is not only smaller but is also reached much faster (i.e., the time constant τ is much smaller).

The observation that the stretching parameter β increases with increasing drain-source voltage indicates that the distribution of the time constants that characterize the trapping and detrapping dynamics during bias stress depends on the drain-source voltage, i.e., the trap distribution becomes more uniform, and hence the response becomes less stretched when the drain-source voltage is increased. Table 2 summarizes the calculated times until 90%, 95%, and 99% of the equilibrium threshold voltage shift is reached for each drain-source voltage. As can be seen, these times decrease by more than four orders of magnitude as the drain-source voltage is increased from 0 to −2 V. Table 2 also confirms that the average time constant $\langle\tau\rangle$ is indeed a more useful metric of the stretched exponential function than the time constant τ.

The finding that the equilibrium threshold voltage shift is much smaller when a drain-source voltage is applied during gate bias stress means that in practical applications of thin-film transistors, such as active-matrix displays and active-matrix imagers, the detrimental effect of the bias stress is less severe, since in these applications a significant drain-source voltage is typically present during transistor operation.

6 Conclusion

The bias stress effect in pentacene thin-film transistors was investigated. It was found that both the equilibrium threshold voltage shift and the time constant of the bias stress-induced threshold voltage shift decrease significantly when a drain-source voltage is applied during the bias stress. This suggests that the drain-source voltage creates a pathway for the fast release of carriers trapped during bias stress.

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